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EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,216	YANG, WENHUA	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 18-37* is/are pending in the application.

4a) Of the above claim(s) *21-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 18-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Summary of changes in this action

1. Claims 1-3, 5-11, 13-15, 18, 20, 29, and 32-37 are newly rejected under 35 U.S.C. 103 (a) as necessitated by Applicant's amendment to claims 1, 8, 15, and 32.
2. Applicant has cancelled claims 4, 12, 16-17, 21-28, and 30-31.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5-11, 13-15, 18, 20, 29, and 33-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spanoche (USPN 6,538,491) in view of Maes et al. (USPN 6,329,848). Spanoche discloses, in Fig. 10, a circuit similar to that claimed, but does not disclose any details regarding the charge pump 623, thus it does not disclose a "transmission gate" composed in the bootstrap (i.e. charge pump) circuit. The reference to Maes et al. discloses, in Fig. 2, a charge pump (i.e. bootstrap) circuit having a transmission gate and receives a buffered input signal. Maes et al.'s bootstrapped charge pump circuit having a transmission gate (TG3 or TG2 of Fig. 2) and a buffered input signal to prevent additional distortion in the output of circuit being

controlled by charge pump. Additionally, the charge pump of Fig. 2 ensures that the output voltage to the gate of the transistor being driven by charge pump is adequate to turn on the transistor by bootstrapping the output of the pump to the buffered input voltage plus the supply voltage. Therefore, it would have been obvious for one of ordinary skill in the art to use the specific charge pump circuit in Fig. 2 of Maes et al. for the generic charge pump of Fig. 10 of Spanoche to prevent unwanted distortion in the output of the charge pump. One would have been motivated to use the specific charge pump circuit in Fig. 2 of Maes et al. for the generic charge pump of Fig. 10 of Spanoche to have a charge pump capable of adequately driving transistors which has reduced distortion at its output.

With respect to claim 1, the above modification discloses, "a multi-stage circuit having a first stage (stage between the phantom lines of Fig. 10 of Spanoche) and a second stage (stage to the right the phantom lines of Fig. 10), the first stage having an output switch (619) and an amplifier (400) with an amplifier output (output of 400), the second stage having an input switch (621) in communication with the output switch (621 is connected to the same node at the output of 400, thus they are in communication with each other), the multi-stage circuit comprising:

a bootstrap module (623, as modified above) in communication with both the output switch and the input switch (623 controls the gates of both 619 and 621 based on the output of 400, thus it is in communication with 619 and 621), the bootstrap module being capable of applying a voltage to both the input and output switches (623 applies voltage to both 619 and 621 to active the switches), the applied voltage ensuring that the first and second switches remain in an on state at specified times (the output of 623

make sure that 619 and 621 remain on during the time period that the output of 623 is higher than the threshold voltage of 619 and 621), the bootstrap module capable of receiving an input voltage at an input (623 (Fig. 2 of Maes et al. discloses as modified above) receives an input voltage at the INPUT node (input to TG3 and TG2)), the bootstrap module having an output to provide the applied voltage (GDRV of Maes et al. applies the output voltage to the gates of 619 and 621 as modified above), the bootstrap module including a transmission gate electrically communicates the input with the output (TG2 communicates the buffered input signal of Fig. 2 to the output GDRV),

a common node between the input switch and output switch (node connected to 400, 619 and 621), the amplifier output coupled to the common node such that there is no intervening switch between the amplifier output and the common node (the output of 400 is directly connected to the common node)."

With respect to claim 2, the above combination discloses, "the multi-stage circuit as defined by claim 1 wherein the input and output switches are controlled to operate at the same phase and duty cycles (clearly the 619 and 621 of Spanoche are controlled to operate at the same phase and duty cycles, because 619 and 621 are controlled by the same signal (output of 623) thus they operate at the same phase and duty cycle of the output of 623.)."

With respect to claim 3, the above combination discloses, "the multi-stage circuit as defined by claim 1 wherein during the specified times, the applied voltage is no less than a minimum turn on voltage required to turn the first and second switches to the on state (clearly when the output of 623 of Spanoche controls 619 and 621 to be

conductive (on) the output of 623 must be large enough (i.e. no less than the minimum) to turn both 619 and 621 on.)."

With respect to claim 5, the above combination discloses, "the multi-stage circuit as defined by claim 1 wherein the bootstrap module includes a charge storage element, the charge storage element (CCP) being capable of storing a constant voltage (CCP stores constant voltage of V), the transmission gate (TG2) coupling the input with the charge storage element to produce the applied voltage at the output (TG2 couples the input voltage to CCP to create a drive voltage GDRV that is equal to the supply voltage plus the buffered input voltage (see Col. 4 lines 53-60)).

With respect to claim 6, the above combination discloses, "the multi-stage circuit as defined by claim 1 further including:

a buffer coupled with the bootstrap module (clearly it can be seen that the charge pump of Fig. 2 of Maes et al. has an buffered input to reduce distortion, thus it obvious that there is a buffer buffering the input connected to the charge pump of Fig 2 of Maes et al. (i.e. 623 of Spanoche as modified above))."

With respect to claim 7, the above combination discloses, "the multi-stage circuit as defined by claim 1 wherein the first stage and second stage comprise a switched capacitor circuit (clearly, the first and second stages comprise switched capacitor circuits, (i.e. 619 with C1 and 621 with C2) which charge capacitors according to the activation state of each switch.)."

With respect to claim 8, the above combination discloses, "a multi-stage switched capacitor circuit comprising:

a first stage (stage between the phantom lines of Fig. 10 of Spanoche) having an output switch (619) and an amplifier (400) with an amplifier output (output of 400);

a second stage (stage to the right the phantom lines of Fig. 10) having an input switch (621) in communication with the output switch of the first stage (621 is controlled by the same output and is activated at the same time as 619, thus it is in communication with 619); and

a bootstrap module (623, as modified above) coupled between both the output switch and the input switch (623 is coupled between 619 and 621), the bootstrap module being capable of applying the same voltage to both the output switch and the input switch (623 applies the same voltage (i.e. its output voltage) to the gates of 619 and 621), the bootstrap module capable of receiving an input voltage at an input (623 (Fig. 2 of Maes et al. discloses as modified above) receives an input voltage at the INPUT node (input to TG3 and TG2)), the bootstrap module having an output to provide the applied voltage (GDRV of Maes et al. applies the output voltage to the gates of 619 and 621 as modified above), the bootstrap module including a transmission gate electrically communicates the input with the output (TG2 communicates the buffered input signal of Fig. 2 to the output GDRV);

a common node between the input switch and output switch (node connected to 400, 619 and 621), the amplifier output coupled to the common node such that there is no intervening switch between the amplifier output and the common node (the output of 400 is directly connected to the common node).

With respect to claim 9, the above combination discloses, "the multi-stage switched capacitor circuit as defined by claim 8 wherein the first stage also includes a

feedback loop coupled with the output switch (619 and C1 comprise the feedback loop)."

With respect to claim 10, the above combination discloses, "the circuit as defined by claim 9 wherein the output switch and the input switch are controlled to operate with the same phase and duty cycle (clearly the 619 and 621 of Spanoche are controlled to operate at the same phase and duty cycles, because 619 and 621 are controlled by the same signal (output of 623) thus they operate at the same phase and duty cycle of the output of 623.)."

With respect to claim 11, the above combination discloses, "the circuit as defined by claim 8 further including a buffer coupled to the bootstrap module (clearly it can be seen that the charge pump of Fig. 2 of Maes et al. has an buffered input to reduce distortion, thus it obvious that there is a buffer buffering the input connected to the charge pump of Fig 2 of Maes et al. (i.e. 623 of Spanoche as modified above))."

With respect to claim 13, the above modification discloses, "the circuit as defined by claim 8 wherein the voltage applied to the input switch is no less than a minimum turn on voltage required to turn the input switch to the on state (clearly when the output of 623 of Spanoche controls 619 and 621 to be conductive (on) the output of 623 must be large enough (i.e. no less than the minimum) to turn both 619 and 621 on.)."

With respect to claim 14, the above modification discloses, "the circuit as defined by claim 8 wherein the wherein the first stage includes a SHA, and the second stage includes an MDAC (it can be seen that the first stage comprises a sample and hold circuit and the second circuit comprises a digital to analog converter in that the both

stages are composed of switched capacitor circuits, which are capable of performing the recited functions (See Col. 1 lines 18-23))."

With respect to claim 15, the above modification discloses, "a multi-stage switched capacitor circuit comprising:

a first stage (stage between phantom lines of Fig. 10 of Spanoche), having a first stage input (input to inverting terminal of 400) a first stage output (output of 400), and an output feedback loop feeding the first stage output back to the first stage input (output of 400, with 619, and C1), the output feedback loop including an output switch (619), the output switch when in an off state interrupting the output feedback loop (when 619 is off, the feed back loop is disabled);

a second stage (stage to the right of phantom lines) having an input switch (621), the input switch in communication with the output feedback loop of the first stage (621 is controlled by the same output and is activated at the same time as 619, thus it is in communication with 619); and

means for applying a bootstrap voltage (623 as modified above) to the output switch and the input switch (623 controls the gates of 619 and 621), the bootstrap voltage maintaining the input switch and the output switch in an on state during a specified time interval (when 623 is activated to output a high voltage 619 and 621 are turned on), the applying means capable of receiving an input voltage at an input (623 (Fig. 2 of Maes et al. discloses as modified above) receives an input voltage at the INPUT node (input to TG3 and TG2)), the applying means having an output to provide the applied voltage (GDRV of Maes et al. applies the output voltage to the gates of 619 and 621 as modified above), the applying means including a transmission gate

electrically communicates the input with the output (TG2 communicates the buffered input signal of Fig. 2 to the output GDRV),

With respect to claim 18, the above combination discloses, "the circuit as defined by claim 15 wherein the output switch and the input switch are controlled to operate with the same phase and duty cycle (clearly the 619 and 621 of Spanoche are controlled to operate at the same phase and duty cycles, because 619 and 621 are controlled by the same signal (output of 623) thus they operate at the same phase and duty cycle of the output of 623.)."

With respect to claim 20, the above combination discloses, "the circuit as defined by claim 15 wherein the first stage includes a SHA, and the second stage includes an MDAC (it can be seen that the first stage comprises a sample and hold circuit and the second circuit comprises a digital to analog converter in that the both stages are composed of switched capacitor circuits, which are capable of performing the recited functions (See Col. 1 lines 18-23))."

With respect to claim 29, the above combination discloses, "the multi-stage circuit as defined by claim 1 wherein a control signal (output of 623) controls the duty cycles of the input and output switches, the input and output switches being controlled to turn on during every rising edge of the control signal (clearly 619 and 621 are NMOS transistors, which are turned on (activated) with a high voltage signal at their gates. Thus, when the output of 623 rises (rising edge) to the threshold voltage of 619 and 621, 619 and 621 will turn on)."

With respect to claims 32-37, all the claim limitations have been considered and it can be seen that claims 32-37 recite the same limitations of claims 1-3, and 5-7. Thus, claims 32-37 are rejected for at least the same reasons as claims 1-3, and 5-7.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gilsdorf et al. (USPN 5,539,351) discloses in Fig. 1 and Fig. 2 a charge pump composed of transmission gates which charge capacitors.

O'Shaughnessy (USPN 5,663,675) discloses in Fig. 5.C a charge pump (bootstrap) circuit that uses a transmission gate to supply an input voltage to a charge storing capacitor to boost the output voltage.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on M-F 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TH
August 28, 2006

LINH MY NGUYEN
PRIMARY EXAMINER